## Amendments to the Drawings:

Please amend the drawings as follows:

In Figure 1, please reference numerals "21" and "23" and associated lead lines;

In Figure 2, please redraw as shown on the enclosed sheet; and

In Figure 4b, please replace reference numeral "20" with reference numeral "21".

In accordance with the Rules, replacement drawing sheets identified in the top margin as "Replacement Sheet" are enclosed. In addition, a marked-up copy of each replacement sheet labeled as "Annotated Sheet" is attached.

Serial No. 10/723,701 Art Unit: 2829

#### <u>REMARKS</u>

The present application has been amended in response to the Examiner's Office Action to place the application in condition for allowance. Applicant, by the amendments presented above, has made a concerted effort to present claims which clearly define over the prior art of record, and thus to place this case in condition for allowance.

### **Drawings**

Figures 1, 2 and 4b have been amended to overcome the Examiner's objections.

Replacement sheets incorporating these revisions are attached, and a marked-up copy of each replacement sheet labeled as "Annotated Sheet" is also attached.

Figure 1 and the specification have been amended to clarify that the contact ring is made up of two portions and one of the portions includes electrical contacts. Figure 2 has been revised to clarify the wafer structure. One having ordinary skill in the art would have readily known that the original Figure 2 was in error because the circuit 38 cannot be provided as being floating off the substrate, and one having ordinary skill in the art readily knows that a wafer is continuous. Figure 4b has been amended to clarify what portion of the contact ring is being depicted.

The Examiner also objected to the drawings contending that "resistance measurement circuitry", etc., as claimed, must be shown in the drawings. In the specification, part 38 is indicated as being reistance measurement circuitry and Figure 2 shows block 38 as being on the substrate. Figure 3 further indicates, in block diagram form, what block 38 is. Block diagrams are acceptable for use with regard to electrical circuits in patent applications (see, for example, Staehelin v. Secher, 24 USPQ2d 1513, 1516 (P.P.A.I. 1992). Applicant respectfully submits that

Serial No. 10/723,701

Art Unit: 2829

Fax sent by 3127048023 TREXLER, ETAL.

the way the specification reads, along with the drawings, as amended, would fully enable one having ordinary skill in teh art to practice the invention without having to perform undue experimentation.

#### Specification

The specification has been amended to incorporate the changes made to the drawings.

#### Claim Rejections

Claims 1 and 12 were rejected under 35 U.S.C. § 102(b) as being anticipated by United States Patent No. 5,894,161 (Akram et al.) and claims 2-11 and 13-18 were rejected under 35 U.S.C. §103(a) as begin unpatentable over Akram et al. in view of United States Patent No. 6,788,082 (Hirao).

The claims have been amdned to more specifically claim the present invention, and to further distinguish the claimed invention from that which is disclosed in the cited references.

Claim 1 now specifically claims a device for measuring resistances associated with electrical contacts, where the device includes a round substrate such that the substrate is configured to mount between a top portion and a bottom portion of a contact ring which is configured for use in a semiconductor wafer electroplating process, a conductive pattern on the substrate, configured to electrically contact the electrical contacts of the contact ring; and resistance measurement circuitry on the substrate and surrounded by the conductive pattern, where the resistance measurement circuitry is connected to the conductive pattern and is configured to not only send test signals to the conductive pattern, but is also configured to receive signals from the conductive pattern and measure the resistances associated with the

Serial No. 10/723,701

Art Unit: 2829

Fax sent by : 3127048023 TREXLER, ETAL. 05-09-06 15:54 Pg: 15/23

electrical contacts of the contact ring. Claim 12 is similar but is directed to a method. Applicant respectfully submits that this is neither disclosed nor suggested by the cited prior art, either alone or in combination.

Akram et al. merely teaches an interconnect 10 having connection pads 28 which connect with a connector 30 which leads to a test circuit 33. Akram et al. neither discloses nor suggests what is being claimed. Akram et al. does not teach a device for measuring resistances associated with electrical contacts, where the device includes a round substrate such that the substrate is configured to mount between a top portion and a bottom portion of a contact ring which is configured for use in a semiconductor wafer electroplating process, a conductive pattern on the substrate, configured to electrically contact the electrical contacts of the contact ring, and resistance measurement circuitry on the substrate and surrounded by the conductive pattern, where the resistance measurement circuitry is connected to the conductive pattern and is configured to not only send test signals to the conductive pattern, but is also configured to receive signals from the conductive pattern and measure the resistances associated with the electrical contacts of the contact ring. Akram et al. Also does not teach or suggest the method which is specifically claimed in claim 12.

Likewise, Hirao also does not teach resistance measurement circuitry on the substrate which is not only connected to the conductive pattern, but which is configured to not only send test signals to the conductive pattern, but also is configured to receive signals from the conductive pattern and measure the resistances associated with electrical contacts of the contact ring.

Serial No. 10/723,701

Art Unit: 2829

Page 12

PAGE 15/23 \* RCVD AT 5/9/2006 4:50:00 PM [Eastern Daylight Time] \* SVR:USPTO-EFXRF-5/1 \* DNIS:2738300 \* CSID:3127048023 \* DURATION (mm-ss):05-24

Fax sent by : 3127048023 TREXLER, ETAL.

contact ring. Hirao fails to disclose or suggest any such testing substrate.

05-09-06 15:54

Pg: 16/23

Unlike what is specifically claimed, the metal plate 102 disclosed in Hirao does not include a conductive pattern thereon, as is claimed in claim 1, or include resistance measurement circuitry which is on the substrate, surrounded by the conductive pattern, and which is configured to not only send test signals to the conductive pattern, but also is configured to receive signals from the conductive pattern and measure the resistances associated with electrical contacts of the

Applicant respectfully submits it certainly does not appear that the circles in the middle of the probe card in Figures 4-8 have anything to do with any contact ring which is being tested.

Instead, it appears that the circles may merely represent, for example, an aperture in the card which makes the card easier to handle without accidentally touching one of the electrodes 5 or 6. Regardless, even if the circles shown in the middle of the probe card in Figures 4-8 can be said to be a "contact ring", there is no indication that the metal plate 102 (identified by the Examiner as being a "substrate") is mountable in a contact ring, or that the metal plate 102 has a conductive pattern or resistance measurement circuitry which is surrounded by the conductive pattern and which is configured to not only send test signals to the conductive pattern, but also is configured to receive signals from the conductive pattern and measure the resistances associated with electrical contacts of the contact ring.

In contrast, while Hirao discloses a "probe card checker", Hirao does not disclose or suggest that the probe card checker both sends test signals and measures the resistances. In fact, Hirao specifically teaches that this is not the case (see Figure 3 of Hirao which indicates current (I) coming in from the top of the diagram, as opposed to coming directly from the probe card

Serial No. 10/723,701

Art Unit: 2829

Page 13

PAGE 16/23 \* RCVD AT 5/9/2006 4:50:00 PM [Eastern Daylight Time] \* SVR:USPTO-EFXRF-5/1 \* DNIS:2738300 \* CSID:3127048023 \* DURATION (mm-ss):05-24

checker 101). According to Hirao, a current is applied to the probe card pins, while the probe card checker checks the resistances associated with each pin (see, for example, col. 5, lines 25-42).

The present application has been amended in response to the Examiner's Office Action to place the application in condition for allowance. Applicant, by the amendments presented above, has made a concerted effort to present claims which clearly define over the prior art of record, and thus to place this case in condition for allowance.

In view of the above amendments and remarks, Applicant respectfully submits that the claims of the application are allowable over the rejections of the Examiner. Should the present claims not be deemed adequate to effectively define the patentable subject matter, the Examiner is respectfully urged to call the undersigned attorney of record to discuss the claims in an effort to reach an agreement toward allowance of the present application.

Respectfully submitted,

Dated: May 9, 2006

James R. Foley, Reg. No. 39,979

TREXLER, BUSHNEEL, GIANGIORGI, BLACKSTONE & MARR, LTD.

105 W. Adams Street, 36th Floor

Chicago, Illinois 60603

(312) 704-1890

965304.WPD

Serial No. 10/723,701

Art Unit: 2829

ANNOTATED SHEET

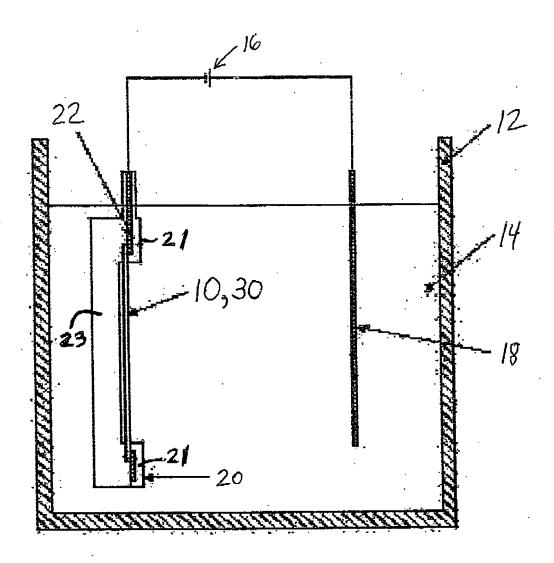


Figure 1

ANNOTATED SHEET

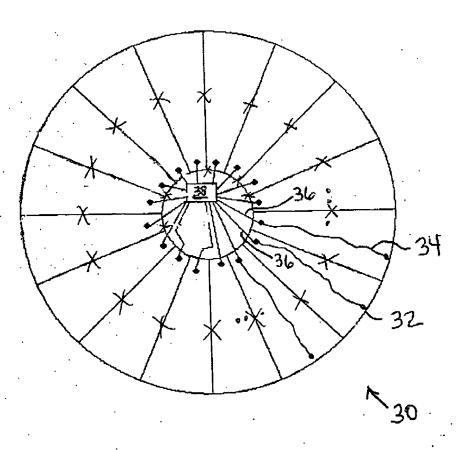
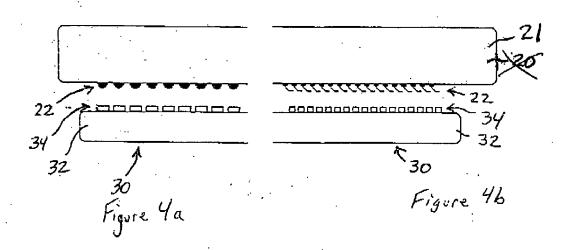


Figure 2

# ANNOTATED SHEET

TREXLER, ETAL.



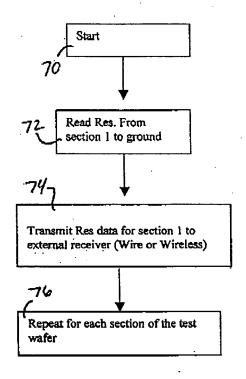


Figure 5